



Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

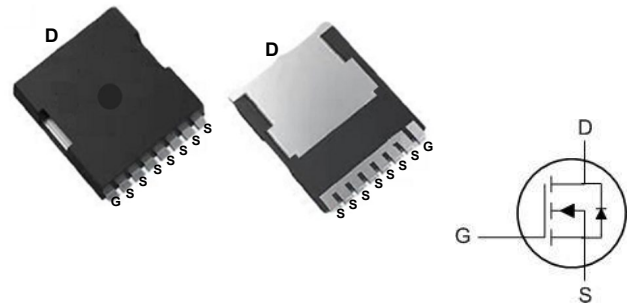
Product Summary

BVDSS	RDSON	ID
60V	1.8mΩ	200A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

TOLL-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	200	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	100	A
I_{DM}	Pulsed Drain Current ²	810	A
EAS	Single Pulse Avalanche Energy ³	352.8	mJ
I_{AS}	Avalanche Current	42	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	96	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	48	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.3	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	---	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =60A	---	1.8	2.4	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	G	G	I	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =10V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =10V, V _{GS} =0V, T _J =100°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =60A	---	8.1	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.8	---	Ω
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =6V, I _D =60A	---	1.1	---	nC
Q _{gs}	Gate-Source Charge		---	0.7	---	
Q _{gd}	Gate-Drain Charge		---	0.4	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DD} =10V, R _G =3Ω, I _D =60A	---	0.7	---	ns
T _r	Rise Time		---	0.7	---	
T _{d(off)}	Turn-Off Delay Time		---	4.0	---	
T _f	Fall Time		---	0.7	---	
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1MHz	---	1.0	---	pF
C _{oss}	Output Capacitance		---	0.1	---	
C _{rss}	Reverse Transfer Capacitance		---	0.1	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	200	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	1.0	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =20A, di/dt=100A/μs	---	56	---	nS
Q _{rr}	Reverse Recovery Charge	μs, T _J =25°C	---	67.5	---	nC

Note :

F The data is tested by surface mounted on a 4-layer FR-4 board with 2oz copper.

G The data is tested by pulsed pulse width ≤ 300us, duty cycle ≤ 2%

 H The EAS data shows Max. Rating at the test condition as V_{GS}=0, V_{DD}=25V, V_{GS}=10V, L=0.4mH, I_{AS}=42A

I The power dissipation is limited by 150°C junction temperature

 J The data is theoretically the same as I_D and I_{DMA}. In real applications, it should be limited by total power dissipation.

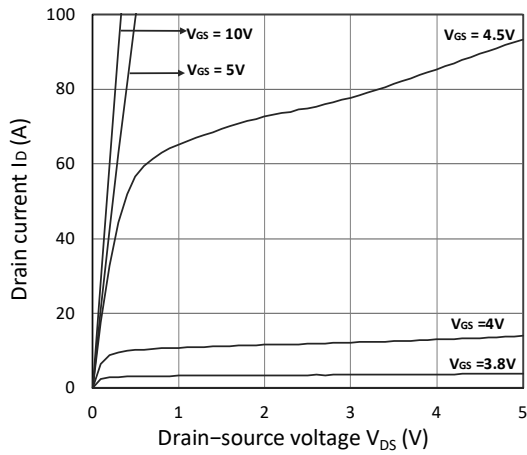
Typical Characteristics


Figure 1. Output Characteristics

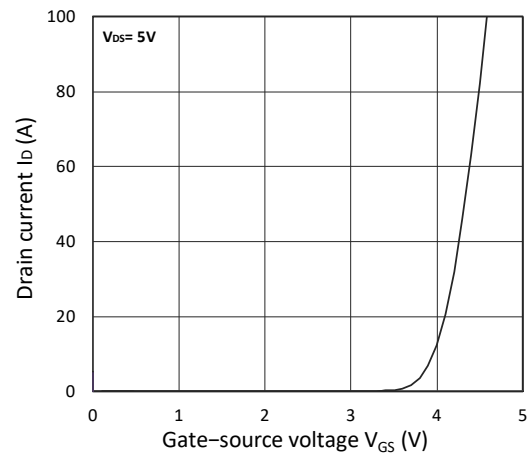


Figure 2. Transfer Characteristics

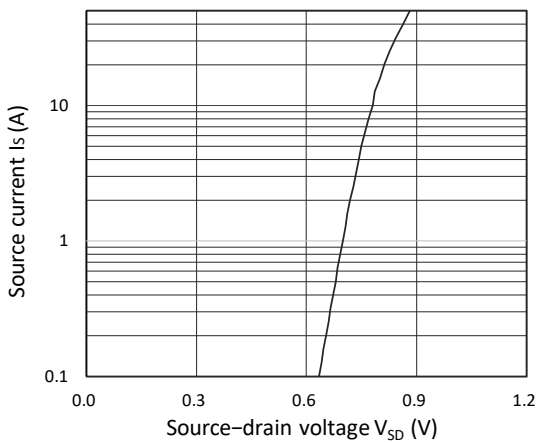
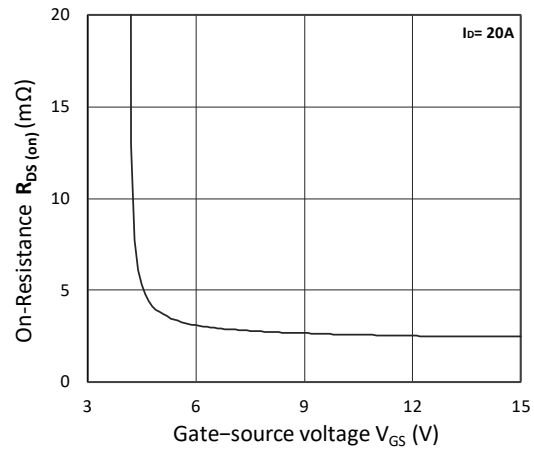
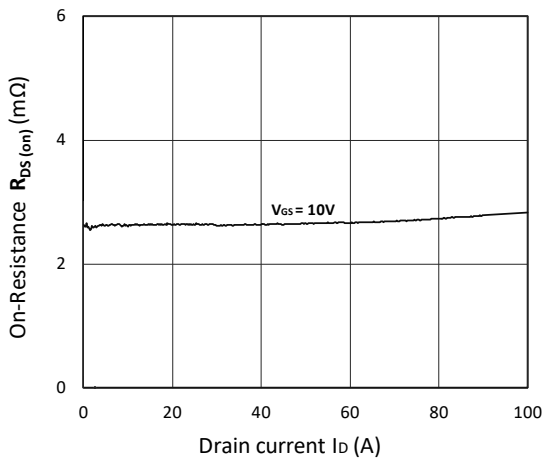
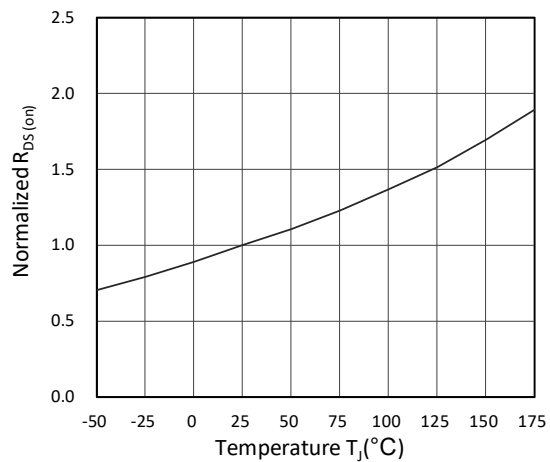


Figure 3. Forward Characteristics of Reverse


 Figure 4. $R_{DS(ON)}$ vs. V_{GS}

 Figure 5. $R_{DS(ON)}$ vs. I_D

 Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

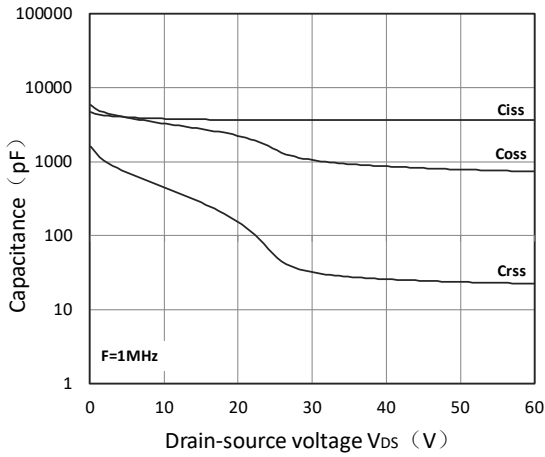


Figure 7. Capacitance Characteristics

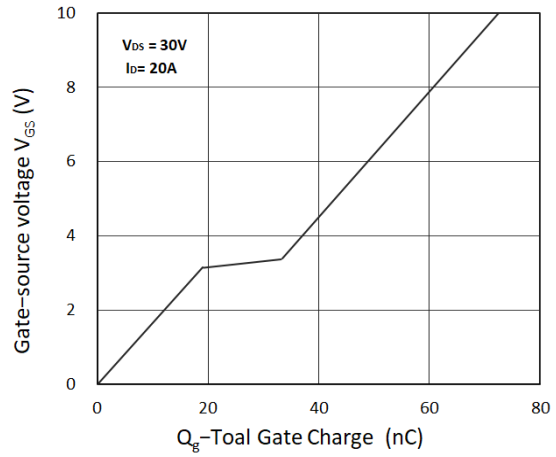


Figure 8. Gate Charge Characteristics

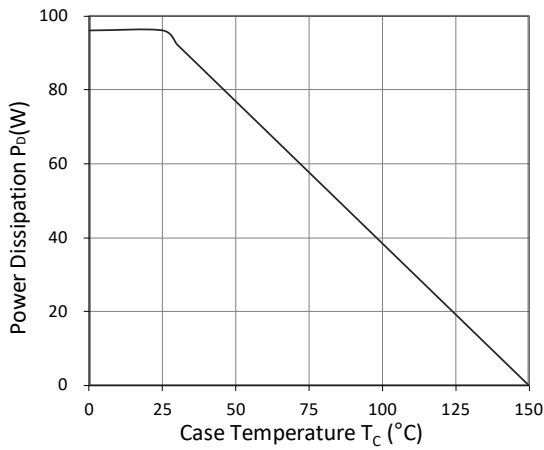


Figure 9. Power Dissipation

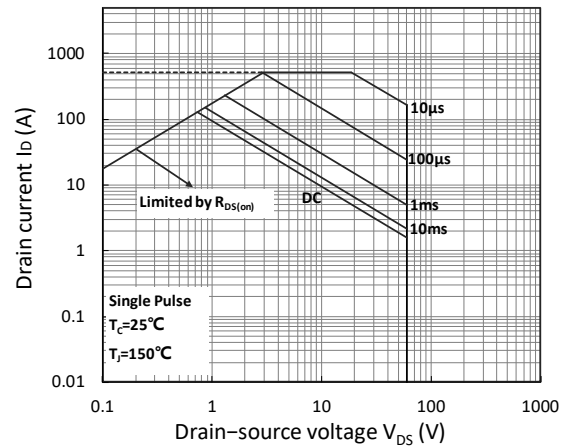


Figure 10. Safe Operating Area

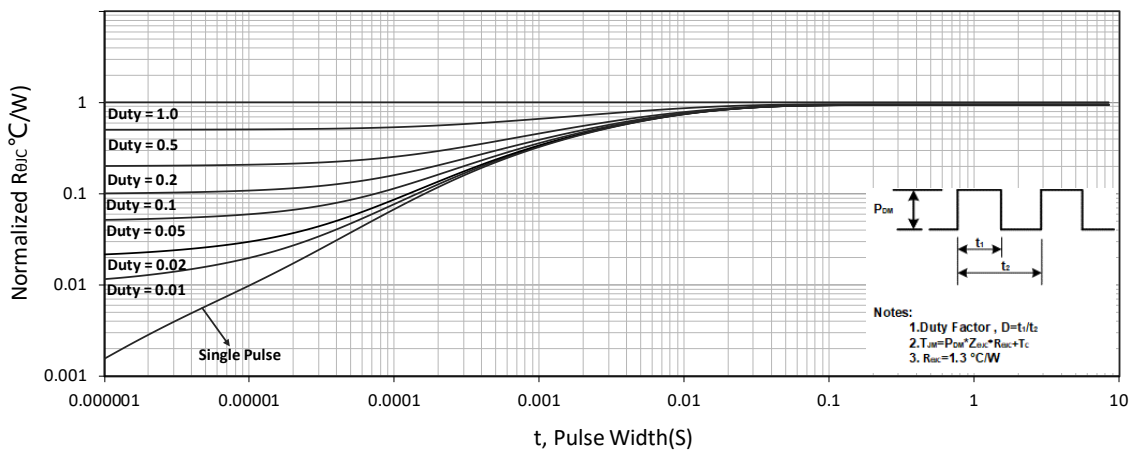
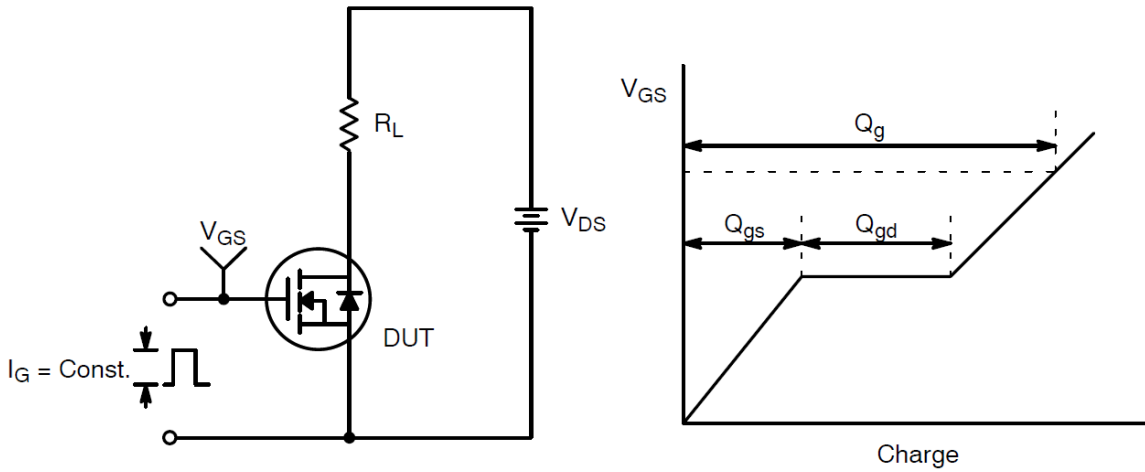
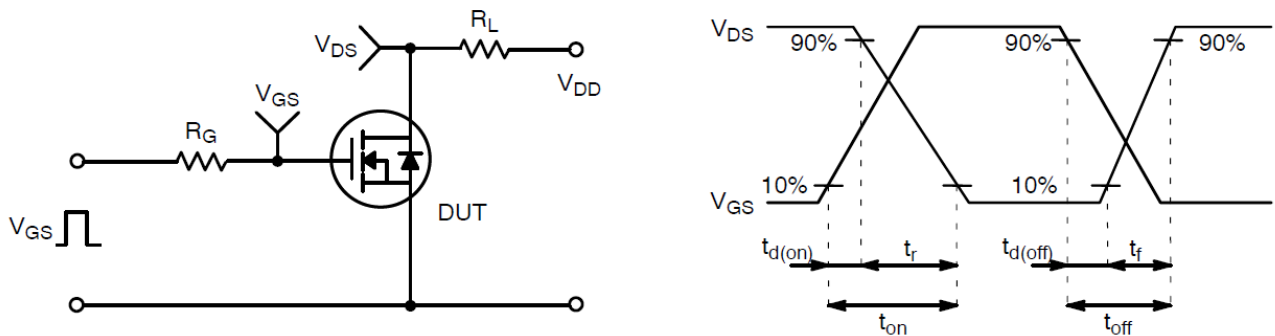
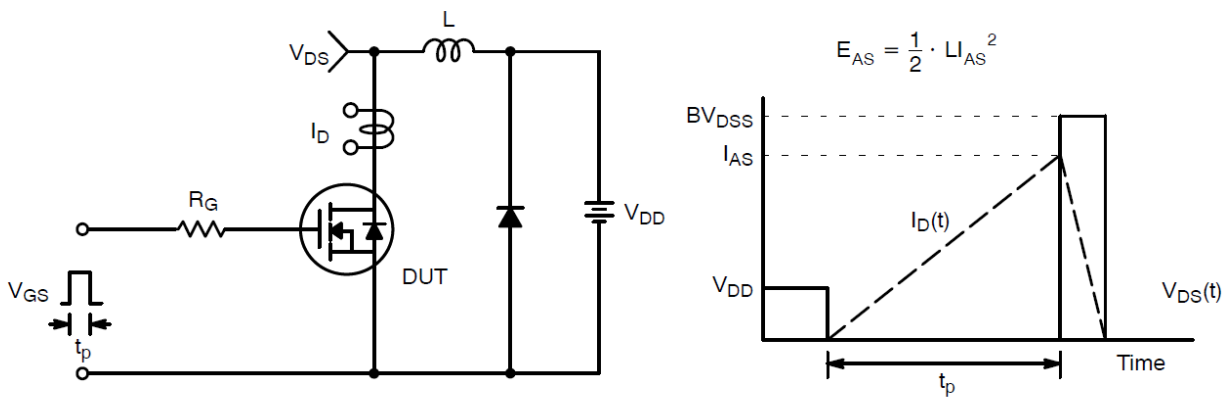
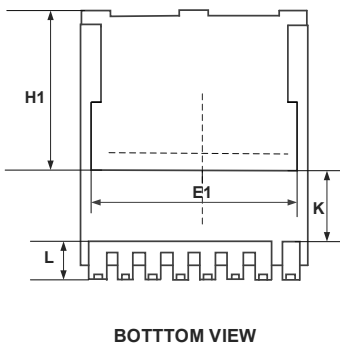
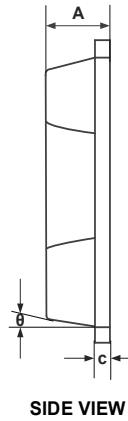
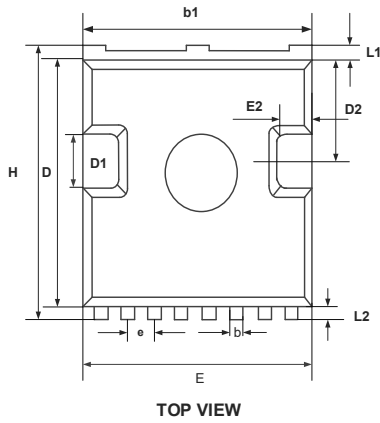


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit and Waveform:

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms

Mechanical Dimensions for TOLL-8L

COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	